

REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 30, 31, and 33-39 are pending in this application. Claims 30, 35, 37, and 39 are amended by the present amendment.

Amendments to the claims find support in the application as originally filed at least in the specification at page 7, line 16 to page 8, line 5, page 10, line 25 to page 12, line 16, page 26, line 19 to page 28, line 3, and page 38, line 15 to page 41, line 10. Thus, no new matter is added.

In the outstanding Office Action dated December 23, 2008, Claims 30, 35, 37, and 39 were objected to; Claims 37 and 38 were rejected under 35 U.S.C. §102(e) as anticipated by U.S. Patent 6,791,112 to Yamazaki et al. (herein "Yamazaki"); and Claims 30, 31, 33-36, and 39 were rejected under 35 U.S.C. §103(a) as unpatentable over Yamazaki in view of U.S. Publication 2003/0008075 to Ueno et al. (herein "Ueno").

Regarding the objection to the claims, Claims 30, 35, 37, and 39 are amended to overcome the informalities noted in the Office Action. Accordingly, it is respectfully requested the objection to the claims be withdrawn.

Furthermore, Applicant respectfully traverses the rejection of Claims 37 and 38 under 35 U.S.C. §102(e) as anticipated by Yamazaki.

Amended Claim 37 is directed to a thin-film transistor that includes, in part an island-shaped silicon layer which is provided on an insulating substrate, a source region and a drain region which are provided with an interval on the silicon layer on the insulating substrate, a gate insulator layer which is provided on the silicon layer between the source region and the drain region, a gate electrode which is provided on the gate insulator layer, and a source electrode and a drain electrode which are provided on the source region and the drain region,

respectively. The gate electrode includes, a first copper diffusion-preventing layer formed on the gate insulator layer, a copper seed layer formed on the first copper diffusion-preventing layer, a copper layer formed on the copper seed layer by an electroless metal plating method, and a second copper diffusion-preventing layer covering an exposed surface including side and upper surfaces of a multilayered structure having the first copper diffusion-preventing layer, the copper layer, and the copper seed layer. A film thickness of the copper layer is greater than that of the copper seed layer. The copper layer has a forward tapered cross section.

According to a non-limiting embodiment of a thin-film transistor according to amended Claim 37, in which a copper layer is formed by an electroless metal plating method laminated on a copper seed layer, it becomes possible to advantageously form a copper film that has an even thickness on the order of nanometers on a TFT substrates of a large size (e.g., 1 square meter) without performing a catalytic processing, for example as in a liquid crystal display. Further, in such a non-limiting embodiment according to Claim 37, since a thick copper layer at the upper layer may have a forward tapered cross section, it becomes possible to advantageously improve the coverage of an interlayer insulation film formed in the upper layer and prevent disconnection and short circuiting of the wiring layer.

Applicant respectfully submits that Yamazaki fails to teach or suggest each of the features of Claim 37. For example, it is respectfully submitted that Yamazaki fails to teach or suggest a copper layer formed by an electroless metal plating method and laminated on a copper seed layer. Furthermore, it is respectfully submitted that Yamazaki fails to teach or suggest that a copper layer of an upper layer having a greater film thickness than a lower layer has a forward tapered cross section.

Yamazaki Figure 1 shows a gate electrode of a TFT including first interconductive layers 113/116 mainly formed of a semiconductor film and provided on a gate insulating film

112. Further, according to Yamazaki, on top of the first inner layer conductive layers 113/116 are laminated second conductive layers 114 and 117 made of copper. Additionally, according to Yamazaki, an outer layer gate electrode made of copper is provided to surround upper and side surfaces of a first gate electrode of the inner layer laminated structure. In other words, the gate electrode of Yamazaki is formed by a complicated trilaminar structure.<sup>1</sup> Thus, Yamazaki includes a structure where the second inner layer conductive layer made of copper is directly laminated on the first inner layer conductive layer formed of a semiconductor film, and accordingly a copper layer made according to the method of Yamazaki may be easily peeled off and may result in poor manufacturing yields due to disconnection. Accordingly, Applicant respectfully submits that Yamazaki fails to disclose or otherwise suggest “a copper layer formed on the copper seed layer by an electroless metal plating method,” as recited in Claim 37.

Furthermore, Yamazaki describes a thin film transistor in which the first inner layer conductive layer of the lower layer, which is formed of a semiconductor layer and has a smaller film thickness than the second inner layer conductive layer of the upper layer, has a forward tapered cross section. Thus, Yamazaki fails to disclose or suggest “a film thickness of the copper layer being greater than that of the copper seed layer [and] the copper layer has a forward tapered cross section,” as recited in Claim 37.

Accordingly, Applicant respectfully submits that Claim 37 patentably defines over Yamazaki.

Therefore, it is respectfully requested the rejection of Claims 37 and 38 under 35 U.S.C. §102(e) be withdrawn.

Additionally, Applicant respectfully traverses the rejection of Claims 30, 31, 33-36, and 39 under 35 U.S.C. §103(a) as unpatentable over Yamazaki in view of Ueno.

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<sup>1</sup> Yamazaki at column 4, lines 27-39.

Amended Claim 30 is directed to a thin film transistor that includes, in part a gate electrode having a first copper diffusion-preventing layer formed by an electroless metal plating method on a gate insulating layer, and a second copper diffusion-preventing layer surrounding an exposed surface including side and upper surfaces of a multilayered structure having a copper seed layer and a copper layer. The copper seed layer and the copper layer have a forward tapered cross section.

In a non-limiting embodiment according to Claim 30, with a copper layer formed by an electroless metal plating method provided on a copper seed layer, a copper film may advantageously be formed having an even thickness on the order of nanometers on a large TFT substrate, without performing a catalytic processing.

Applicant respectfully submits that Yamazaki and Ueno fail to teach or suggest the features of amended Claim 30.

According to Yamazaki, a cross section of a thick second inner layer conductive layer of an upper layer is rectangular. Therefore, Applicant respectfully submits that in a thin film transistor according to Yamazaki there may arise a problem in the coverage of interlayer insulation film formed in the upper layer resulting in disconnection and short circuiting of the wiring layer which would reduce manufacturing yields. Additionally, as discussed above, Yamazaki describes a thin film transistor having a first inner conductive layer of a lower layer which is formed of a semiconductor layer and has a smaller film thickness than a second inner layer conductive layer of an upper layer, and according to Yamazaki, the first inner layer conductive layer of the lower layer has a forward tapered cross section.

Accordingly, Applicant respectfully submits that Yamazaki fails to teach or suggest a copper seed layer and copper layer that have a forward tapered cross section according to independent Claim 30.

Further, in a device according to Yamazaki, in which a copper second inner layer conductive layer is directly laminated on a first inner layer conductive layer formed of a semiconductor film, the copper layer of Yamazaki may be easily and disadvantageously peeled off, resulting in poor manufacturing yields.

Applicant respectfully submits that Ueno fails to supply the features of Claim 30 lacking in the disclosure of Yamazaki. For example, Ueno discusses a device in which copper wiring is used as a wiring layer, and Ueno fails to disclose or suggest the use of copper layers in a semiconductor device, which presents additional problems regarding deterioration of characteristics due to dispersion of copper. In particular, Ueno discusses that

in case that a wiring layer is made of Cu (copper), Cu constituting the wiring layer diffuses into an insulating interlayer so that it may bring about bad insulation. Therefore, it is indispensable to interpose a diffusion prevention layer between the wiring layer and the insulating interlayer and thereby prevent Cu from diffusing into the insulating interlayer.

... [I]n case that the wiring layer 1 is formed on this diffusion prevention layer by electroplating, in particular, with copper, since the diffusion prevention layer of TaN, TiN, or the like, as described above, is inferior in electrical conductivity, a Cu seed layer or the like as a conductive layer is required.<sup>2</sup>

Furthermore, according to Ueno FIGs. 1-4, a wiring layer 11 has a rectangular cross section.

Accordingly, Applicant respectfully submits that Yamazaki and Ueno fail to teach or suggest “a copper seed layer in which an undesired portion is removed on the first copper diffusion-preventing layer [and] a copper layer formed on the copper seed layer of which the undesired portion is removed, the copper layer being formed by the electroless metal plating method and a film thickness of the copper layer being greater than that of the copper seed layer ... wherein the copper seed layer and the copper layer ... have a forward tapered cross section,” as recited in independent Claim 30.

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<sup>2</sup> Ueno at paragraphs [0005]-[0006].

Furthermore, Applicant respectfully submits that Yamazaki and Ueno also fail to disclose or otherwise suggest “a first copper diffusion-preventing layer formed by an electroless metal plating method on the gate insulator layer; a copper seed layer in which an undesired portion is removed on the first copper diffusion-preventing layer; a copper layer formed on the copper seed layer [and] being formed by the electroless metal plating method,” as recited in independent Claim 30.

Accordingly, Applicant respectfully submits that Claim 30 and claims depending therefrom patentably define over Yamazaki and Ueno.

Claim 35 is directed to a thin-film transistor that includes, in part, a source electrode and a drain electrode that comprise a first copper diffusion-preventing layer formed on the source region and the drain region; an organometallic compound material layer having a forward tapered cross section formed on the first copper diffusion-preventing layer by removing an undesired portion; a copper layer having a forward tapered cross section formed on the organometallic compound material layer of which the undesired portion is removed; and a second copper diffusion-preventing layer covering an exposed surface including side and upper surfaces of a multilayered structure having the first copper diffusion-preventing layer, the copper layer and the organometallic compound material layer. The organometallic compound material layer and the copper layer have a forward tapered cross section and are surrounded by the first copper diffusion-preventing layer and the second copper diffusion-preventing layer.

For reasons similar to those discussed above, Applicant respectfully submits that Yamazaki and Ueno fail to teach or suggest the features of Claim 35. For example, Yamazaki discusses a trilaminar structure including a titanium film, an aluminum film containing titanium, and a titanium film, which is different than the structure recited by Claim 35. For example, Applicant respectfully submits that Yamazaki is silent regarding forming a

copper layer on a source electrode and a drain electrode. Ueno describes using a copper wiring as a wiring layer and fails to disclose or otherwise suggest the claimed features lacking in the disclosure of Yamazaki. For example, Ueno is silent regarding the application of copper wiring layer in a semiconductor device that has a problem in the deterioration of characteristics due to dispersion of copper.

Accordingly, Applicant respectfully submits that Claim 35 also patentably defines over Yamazaki and Ueno.

Claim 39 is directed to a thin-film transistor that includes a source electrode and a drain electrode comprising a first copper diffusion-preventing layer formed on the source region and the drain region; a nickel seed layer or a seed layer made of a metal material of group VIIIa including a cobalt seed layer which is formed on the first copper diffusion-preventing layer and of which an undesired portion is removed, the undesired portion being a portion other than an area where the source region and the drain region are formed; a copper layer formed on the nickel seed layer or a seed layer made of a metal material of group VIIIa including a cobalt seed layer; and a second copper diffusion-preventing layer covering an exposed surface including side, upper and lower surfaces of a multilayered structure having the nickel seed layer or a seed layer made of a metal material of group VIIIa including a cobalt seed layer and the copper layer. The nickel seed layer or a seed layer made of a metal material of group VIIIa including a cobalt seed layer and the copper layer are surrounded by the first copper diffusion-preventing layer and the second copper diffusion-preventing layer, and have a forward tapered cross section.

Applicant respectfully submits that Yamazaki and Ueno also fail to teach or suggest the features of Claim 39 for reasons similar to those discussed above.

Accordingly, it is respectfully submitted that Claim 39 also patentably defines over Yamazaki and Ueno.

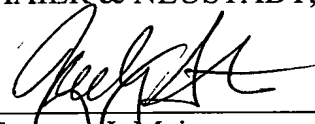
Therefore, Applicant respectfully requests the rejection of Claims 30, 31, 33-36, and 39 under 35 U.S.C. §103(a) as unpatentable over Yamazaki in view of Ueno also be withdrawn.

Accordingly, it is respectfully submitted that independent Claims 30, 35, 37, and 39, and claims depending therefrom, are allowable.

Consequently, in light of the above discussion and the present amendment, this application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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